TECHNOLOGY

DIGITAL MODULATION AND CLASSIFICATION OF BASEBAND SIGNALS USING TMS320C6701 DSP

Abdullah ÇAVUŞOĞLU*   Mustafa SERT**
*Gazi University, Technical Education Faculty, Ankara, Turkey
**Baskent University, Department of Computing Science, Ankara, Turkey

ABSTRACT

In this study, a real-time software modem is developed. TMS320C6701, a powerful DSP microprocessor is used in the designs. Nato Stanag 4285 standards are used in the modem software. Appropriate channel equalization methods are tested and used to enable the software to operate even under the HF band distortion. Control and interface software are developed to integrate DSP and PC system. The number of analog parts is reduced to minimum to reach the target of developing both the transmitter and the receiver parts with software on the DSP. The RF parts are the location for the analog parts, starting from the IF part the signals are processed by software. Therefore, all the synchronization, equalization operatio+ns are realized digitally. These structures, called software radio, have been gaining importance in the recent years and are going to be used in modern digital radio, TV and similar systems.

Key Words: Digital modulation, TMS320C6701 DSP, Modems

TMS320C6701 İŞLEMCİSİ KULLANILARAK SAYISAL MODÜLASYON GERÇEKLEŞTİRİLMESİ VE TABANBAND SİNYALLERİNİN SINIFLANDIRILMASI

ÖZET

Bu çalışmada gerçek zamanlı modem yazılımı geliştirilmiştir. TMS320C6701 tasarımlarda kullanılan güçlü bir DSP mikroişlemcisidir. Yazılımda Nato Stanag 4285 standardı kullanılmıştır. Uygun kanal eşitleme metotları test edilerek kullanılmış ve yazılımın HF bandındaki bozulmalarda dahi çalışabilmesi sağlanmıştır. DSP' nin kişisel bilgisayarlara entegrasyonu için control ve arayüz yazılımları geliştirilmiştir. Kullanılan analog parçaları en aza indirgenerek hem gönderici ve hem de alıcı kısmın tamamen DSP üzerinde yazılımla gerçekleştirilmesine imkan sağlanmıştır. Analog parçaların yer aldığı RF kısmının IF bölümünden başlamak üzere sinyaller yazılımla işlenmiştir.Tüm senkronizasyon, eşitleme işlemleri dijital olarak gerçekleştirilmiştir. Yazılım radyosu olarak adlandırılan buradaki yapılar son yıllarda önem kazanmışlardır ve modern dijital radio sistemlerinde ve benzeri TV sistemlerinde kullanım alanı bulacaklardır.

Anahtar Kelimeler : Sayısal modülasyon, TMS320C6701 İşlemcisi, Modemler

1. INTRODUCTION

Developing communication technologies and the development of different modulation techniques in various frequency ranges raises the requirement of applying the new techniques in the transmitter/receiver systems. Parallel to these developments we see the conversion of analog systems into digital systems, which makes the digital, design of transmitter/receiver systems a necessity. To be able obtain a fully digital system; the starting point is carrying all of the base band transmitter/receiver operations into digital medium. Therefore a simple re-programming makes it possible to get different communication systems and the future improvements could be realized in very short time scale. In addition, the size of the equipment is reduced. To achieve this flexible structure, the first step is designing a digital modem.

In our implementation to demodulate base band PAM, BPSK and QPSK digital modem signals we used synchronization and channel-equalization algorithms, for High Frequency (HF) receiver modems the developed system complies with the NATO Stanag 4285 standards. For the developments we used TMS320C6701 digital signal processor for real time application. The TMS320C6701 processor draws too much current which makes it unsuitable for mobile applications where batteries are used as the power source. In such cases the processor could be replaced with a TMS320C54x family processor. We have developed our software under TMS320C6701 assembly language. In section 2 the development of the modem structure is presented. In section 3 the software that has been developed for the modems' receiver/transmitter mode applications has been summarized. While in section 4 the hardware details of the TMS320C6701 signal processor which is used in real time applications has been reviewed. The performance of the developed system and results are summarized in section 5.

2. MODEM ARCHITECTURE

General information about modem architectures can be found at references [3, 4, 5]. The modulation and demodulation characteristic, which has been used in this study and defined in Nato Stanag Standard 4285, is summarized in section 2.1.

2.1 Modulation

The modulation technique, which is defined in Nato Stanag 4285, is provided shifting the phase of a base-band 1800 Hz carrier signal. This base-band signal is then transmitted through the desired frequency by shifting this signal to RF. The modulation speed is 2400 bauds and modulation resolution is 10^{-5}. The resolution of the oscillatory that produces 1800 Hz carrier is also 10^{-5}. The phase shift of the modulated signal relative to the unmodulated reference sub-carrier may take one of the phase values corresponding to the PSK modulation [3].

A signal that has been modulated by an 1800 Hz sub-carrier is required to involve a 3000 Hz bandwidth. Raised cosine transmitter/receiver with roll-off 0.2 is used to achieve this goal. The frame structure of it is shown in Figure 2.
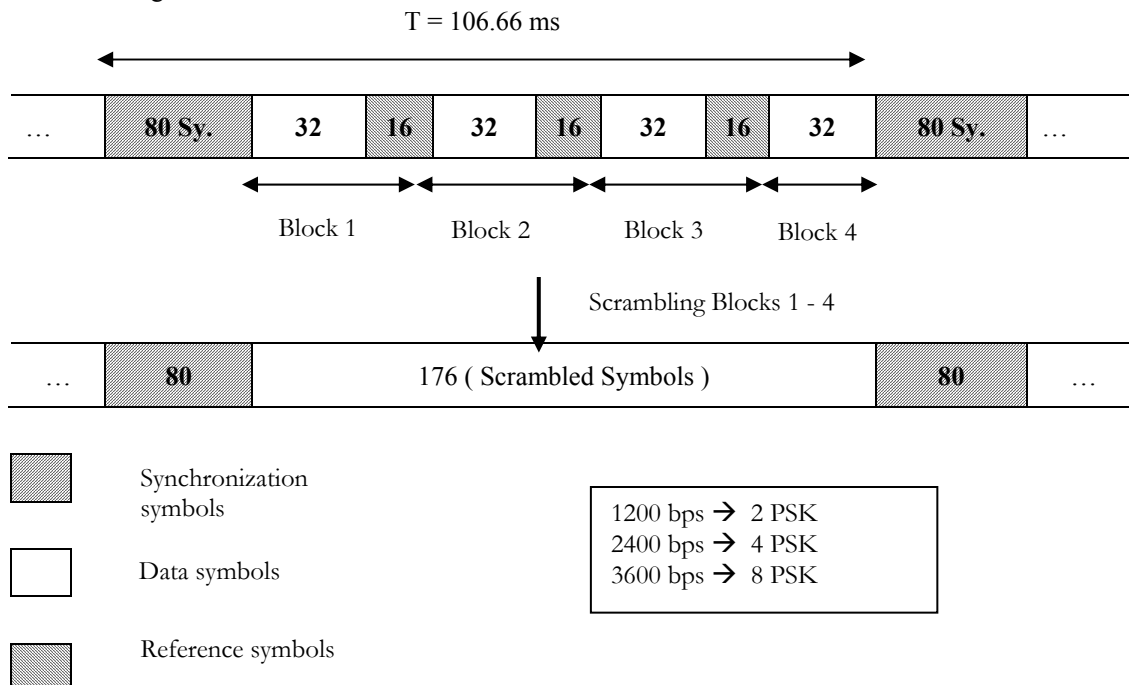
Figure 2. Frame structure.

The symbols to be transmitted are structured in recurrent frames of 106, 6 ms in length. The numbers of bits transmitted per frame are 128 at 1200 bps, 256 at 2400 bps and 384 at 3600 bps. A frame consists of 256 symbols. Eighty of these symbols are for synchronization, 48 of them are for reference, and remaining 128 are data symbols. Long 'one' and 'zero' sequences are prevented by mixing reference and data symbols with the sequences generated by the scrambler [3]. The scramble generates a PSK sequence of 8 phases. Thus, an

8-PSK signal is transmitted through the transmitter, whatever the data rate may be (1200, 2400, or 3600 bps). Doppler shift, symbol synchronization, and equalizer training is provided by using modem synchronization sequence.

3. MODEM SOFTWARE

The signals received from the communication channel need to be processed using signal processing techniques at side of the receiver modem. In the modem structures the transmitter modem software is generally standard and simpler when compared to the receiver modem. In other words the receiver parts of the modems are generally more complex and contain time-consuming operations than the transmitter parts [1]. Therefore in this study we emphasized on the receiver modem. The receiver modem software basically consists of three parts: the first is the signal recognition part. This is done by the use of preamble arrays periodically send by the transmitter [3]. Secondly, the bit and phase synchronization operations are performed by the use of numerical phase-lock loops. In the last part, equalization and array recognition operations are performed against the irregularities of the flow within the channel. This part is the most important section of the receiver structure. In this part depending on the equalization or the recognition technique – channel estimation or inverse channel estimation – the system performance can be better.

The analog signal, which has been sampled at a fixed frequency rate at analog/digital converter, goes through a clock synchronization block. The main aim of this block is to find the differences between the transmitter and receiver clocks and to restore these differences. The selection of the algorithm to be used here is critical, because it effects the overall performance of the receiver modem. The output of the clock synchronization is brought to zero-frequency level by the base band carrier signal. At the same time, with the frequency correction operation errors due to frequency differences are corrected. The channel equalization part removes the effects of the channel. Before the channel equalization, the starting point of the envelope is found. This operation is performed with the link between the synchronization sequence and the envelope.

3.1 Timing Recovery

Timing difference between transmitter and receiver has to be removed. Unless this operation is performed with great care the receiver modem shall not be able to get the information send by the transmitter modem in good shape. Since the transmitter signal is being exposed by the communication channel's noise and distortion effects, the sample points of the transmitted signal has to be determined correctly at the receiver side to obtain the transmitted digital information.

It is an important step to obtain the time reference and correct sample points from the corrupted signal. Nonlinear Spectral Line algorithm is used to detect the timing error [14]. This algorithm is shown in Figure 3. This algorithm works more efficient in complex channels [8]. The main idea in this method is to produce a timing tone by taking the signal via a nonlinear unit at the symbol frequency. A frequency offset estimation mechanism is added to this method. The first step in this algorithm is to take the square of the received signal. Then this signal is multiplied by $e^{-j2\pi m/L}$ and a summation is performed. Loop filter is a low-pass filter and is used to provide clarify the error information. Phase value is determined by using both arc operator and loop
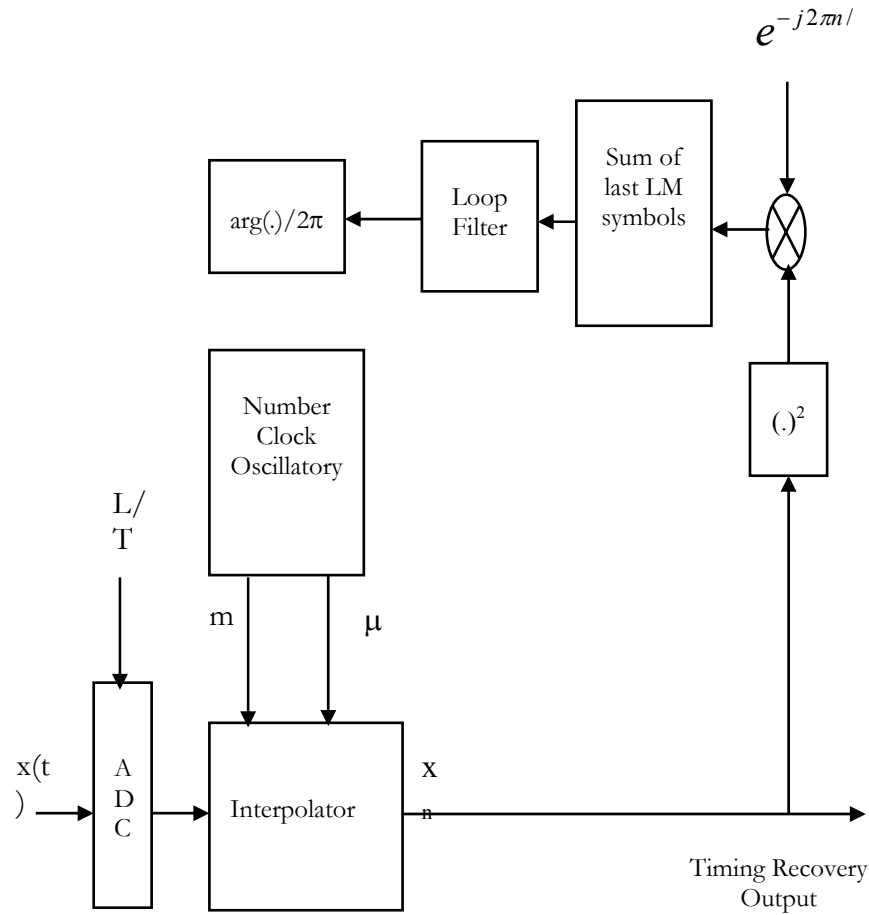
$$e^{-j2\pi n l}$$

Figure 3.Feed-back timing recovery

filter output. Thus the obtained phase information is used to determine the interpolator's parameter. The L, is a value used in the algorithm as the additional sampling factor. Number Clock Oscillatory (NCO) is used instead of the Voltage Controlled Oscillatory (VCO) in the case of the digital versions of the feedback algorithms. NCO produces two arguments. The first parameter μ is used to calculate interpolator's filter coefficients, and m is used to determine the symbols that will enter to the operation.

The timing recovery algorithm works as follows: After providing sampled signals, the correct sample values are formed at the interpolator block and the incorrect values are ignored. At this stage, the obtained results are used to form the output values. However the errors on the signal should be detected to control the interpolator. At this point, m defines the error index of the samples while μ is then used to correct the parameter m. These estimated parameters (μ and m) are effective on the interpolator and are updated for each new samples of the iteration. The error that has been calculated at this stage is obtained for the derivative of a single argument function on discrete-time case. This error signal shows whether the function provided by the derivative is increasing or not, and also the slope. To overcome the abrupt high derivative effects, the output of the relevant block is filtered to preserve the system stability.

3.2 Channel Equalization

One of the most important problems in any practical channel is the spreading of individual data symbols passing through the channel due to inevitable filtering effect. For consecutive symbols, this spreading causes part of the symbol energy to overlap with neighboring symbols, causing Inter Symbol Interference (ISI). ISI can significantly degrade the ability of the data detector to differentiate a current symbol from diffused energy of adjacent symbols. Even with no noise present in the channel this can lead to detection errors [9]. These effects should be removed at the receiver modem. This channel effect can also be the channel distortion. In linear communication channels, the transmission of digital signal is limited by ISI. To control it, time reaction of the channel should be controlled. In communication systems the mechanism that is used to

prevent the ISI is called equalizer [2]. In this study decision feedback equalizer is used to overcome the ISI. Decision feedback equalizers are appropriate for the HF channels as described in [3]. A typical decision feedback equalizer is shown in Figure 4.

Training sequences are transmitted periodically from the transmitter according to the frame structure as defined in NATO Stanag 4285. Then, decision feedback equalizer is being trained by using this sequence.

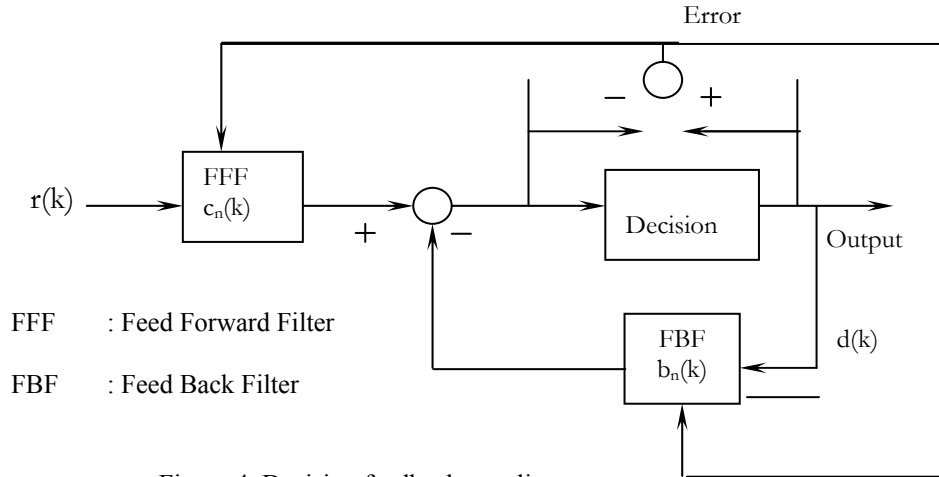FFF   : Feed Forward Filter

FBF   : Feed Back Filter

Figure 4. Decision feedback equalizer

Decision feedback equalizer removes the effects of the preceding symbols by using a feedback filter. FFF and FBF equations are shown in Equation 1 and Equation 2 respectively. Here, α defines both converging rate of the DFE and the energy of the error.

$$c_n(k+1) = c_n(k) - \alpha e_k r_{k-n}, \, n = 0,1,..., \, N-1 \tag{1}$$

$$b_n(k+1) = b_n(k) - \alpha e_k d_{k-n}, \, n = 0,1,..., \, N-1 \tag{2}$$

4, HARDWARE ARCHITECTURE

TMS320C6701, a powerful DSP microprocessor is used to implement the real time system. Hardware configuration of the DSP consists of two modules. These are the digital signal processor (Heron1) and the A/D converter (Hegd1) modules. These modules are fitted to the carrier card, and the carrier card is fitted to the PCI interface.

The modules on the carrier card communicate with each other via the registers, that is, carrier card has its point-to-point connections between module sites provided by fixed bi-directional FIFOs. Each FIFO is 32-bits wide, but can switch into a 16 bit wide mode if a 16-bit module is detected by the hardware [6].
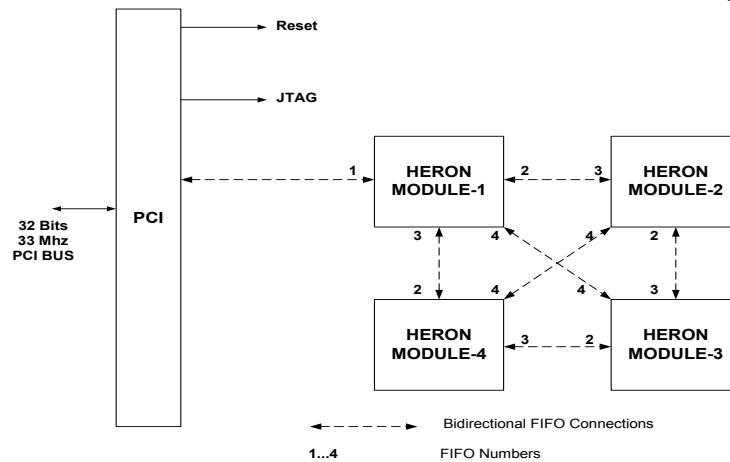

Figure 5. Connectivity of the FIFOs on the HEPC8.

In our configuration, there is one Heron1 module and one Hegd1 module on the HEPC8. Heron1 module holds the C6701 processor, and the Hegd1 module holds the 3 MHz 12 bit A/D converter. This configuration may change according to the applications type. In this case, the user configures the board number switch of the HEPC8. In our study, this configuration set to the 0 and is used to access board through the API software [7]. We used Hunt Engineering API software to communicate between the PCI interface of the HEPC8 and the host machine software. We also used to provide standard I/O access to the host machine's I/O devices from within our DSP program. The software structure between the host machine and the DSP card is shown in Figure 6. This API software consists of a driver layer and a library layer.
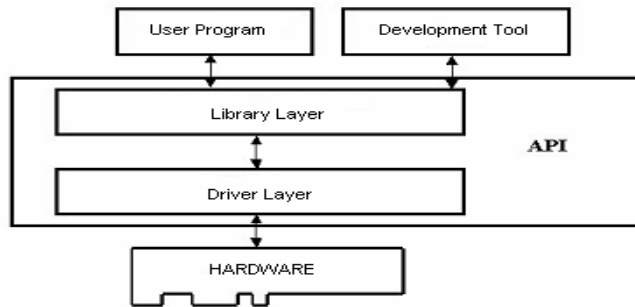

Figure 6. Hunt Engineering API

Our algorithms are written in the C programming language. The DSP program consists of the modem algorithms and the communication functions. The program was compiled using TI Code Generation Tools and then the developed   software was uploaded onto the DSP. A text based configuration file, which can be considered as a map file is used to define which programs, should be loaded onto which processor and memory.

4.1   Real-Time System

For the real time implementation, we generated PAM, BPSK, and QPSK signals in different characteristics using Matlab. Then these signals are sampled at 8 KHz and transferred to the analog media. The characteristics of the generated signals are shown in Table 5.

Table 5. BPSK and QPSK characteristics

Modulation Type	BPSK (1 bit) 2^1		QPSK (2 bit) 2^2			
Input	0	1	00	01	10	11
Output	$(+/-)\sin(2\pi f_o t + \phi)$		$(+/-)\sin(2\pi f_o t + \phi)$ $(+/-)\cos(2\pi f_o t + \phi)$			

Then, we applied the analog signals to the TMS320C6701's input channels. These signals are sampled using A/D converter. We used the double buffering algorithm to achieve real-time processing. The output of the converter consists of complex data, that is, each sampled value includes some other information. One of them is the channel number. So unnecessary information is cleaned and the real signal data is taken. These values are stored in a buffer and applied to the DSP software. The DSP software processes the data and produces the output. These outputs are then transferred to the host machine's memory to visualize the results.

5. SYSTEM PERFORMANCE AND THE EXPERIMENTAL RESULTS

In Figure 7.a a base band QPSK signal is simulated. To see the achievement of the symbol synchronization algorithm the QPSK baseband signal with distorted symbol synchronization have been simulated. The triggering difference between the transmitter and receiver is given as $0 \leq t_0 \leq 1$. If the t_0 goes towards zero we get smaller sampling clock rate difference between the transmitter and receiver. However if we get a result nearing to '1' then this means we have a greater difference between them (figure 7b).

In this context, the developed time synchronization algorithm have successfully calculated the simulated QPSK base band signal's symbol synchronization triggering time. Afterwards, within the time domain this triggering time has been altered, as it can be viewed from the figure 8a the algorithm has successfully followed these alterations.
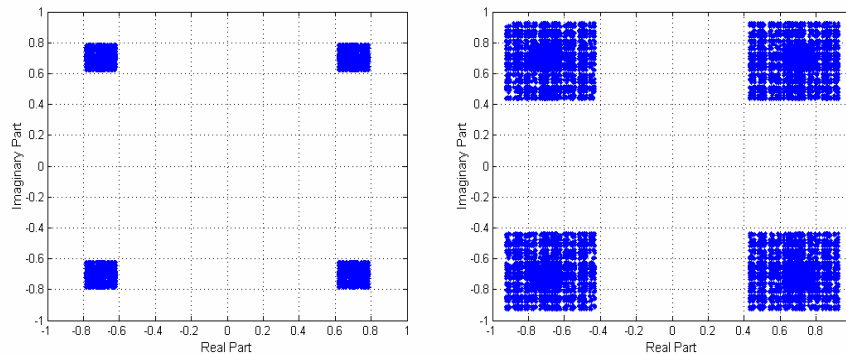

Figure 7. The QPSK Data with t_0=0,2 (a) and t_0=0,6 (b) (without channel effect)

At the Figure 8 time synchronization output for the QPSK signal with the clock difference given in figure 7 is presented.
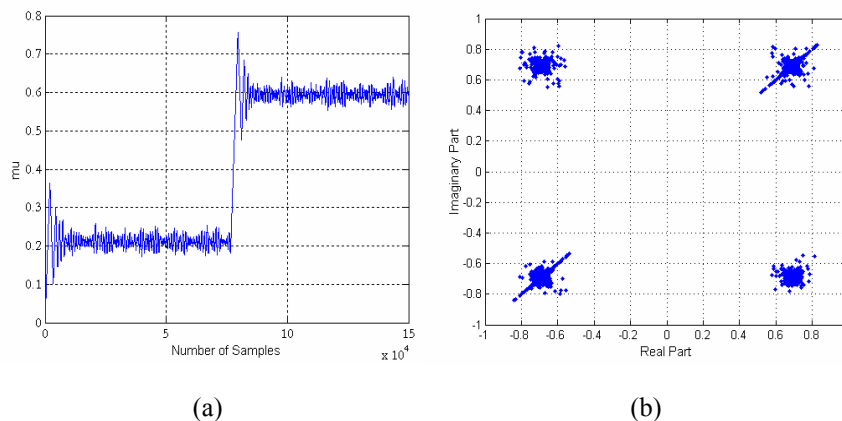

(a)   (b)

Figure 8. (a)The continuous follow-up of the phase difference between the transmitter and the receiver: to=0,2 and to=0,6 (b) The output of the time synchronization algorithm which corrects the phase difference of the sampling clocks of the transmitter/receiver.

As seen from the figure 8 the clock reference differences of the sampled frequencies of the transmitter and receiver continuously monitored and gathered at the right regions.

Without the channel effect, when there is no sampled reference clock difference of the generated QPSK between the transmitter/receiver produces a sharper gathering as seen at figure 9a.

With the channel effect and differing reference clocks of the transmitter/receiver produces the results shown at figure 9b. The channel effect and differences at triggering times causes the transmitted symbols to be mixed with each other. To overcome this problem a decision-based feedback equalization algorithm is used. This algorithm uses the linear filter output to estimate the error between the input/output signals. This error signal is then minimized to find the equalization filter coefficient. A perfect filter produces the original input signal as the output; hence the error term is zero. However this is practically impossible. When we get a term nearer to zero then this means the algorithm is working without any problems. The algorithm finds the values of instant signals that has been transmitted and differentiates the ISI effect and adds it to the forthcoming values.

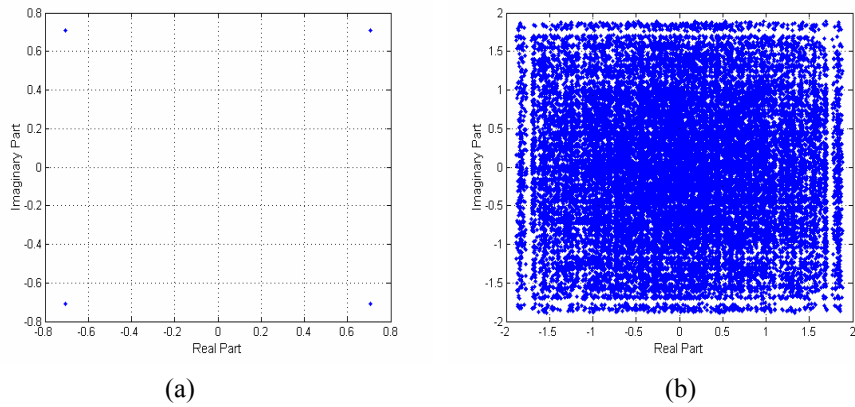(a)   (b)

Figure 9. QPSK data: No channel effect and phase difference between the Transmitter/Receiver sampling clocks (a). QPSK data having timing error and channel effect Channel = [0.2 0 0 0 0.1 0 0 0 0.3 0 0 0 1 0 0 0 0.6 0 0 0 0.4] (b).

In figure 10a the result of QPSK (with channel effect and triggering errors) after being subjected to the clock synchronization algorithm has been presented. In this case the algorithm correctly finds the varying triggering errors in the time and can follow varying triggering time difference. For the QPSK signal given in Figure 9b the clock synchronization algorithm produces the output given at figure 10b. The effect of ISI on the signal passing through the communication channel is devastating (Figure 9b) when the sampling clock differences of the transmitter and receiver are taken into considerations. To solve this problem we developed an equalization algorithm, which improves the signal as shown at Figure 11a. The real part of this signal is seen at figure 11b.
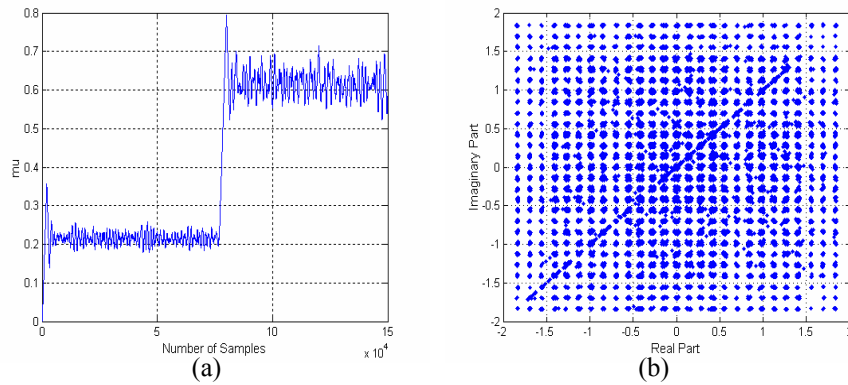

(a)   (b)

Figure 10. The continuous monitoring of the sampled clock differences between the transmitter/receiver: to=0,2 and to=0,6 (a) Digital clock synchronization –correcting the phase differences – output of the sampled receiver and transmitter clocks (b).
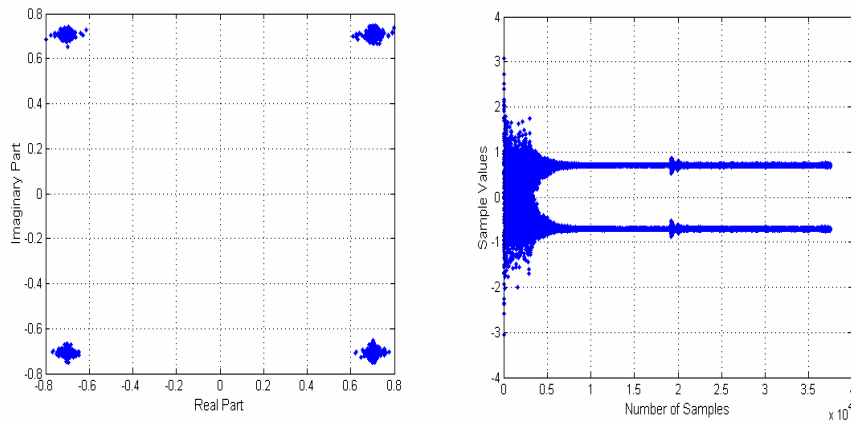

Figure 11. Decision feedback equalization output (a)

5. RESULTS AND CONCLUSIONS

In this study, a digital modem with the clock synchronization decision feedback equalization algorithms have been developed and tested. The behavior of the algorithm against distortion phase errors and various other conditions have been given. The algorithms have been developed on TMS320C6701 microprocessor and a special software developing tool has been used. And real data has been for the real time tests. HF frequency range and wired modem data has been used with different distortion and channel models for the tests. The DSP board and host PC communication software and user interfaces also have been developed to provide a test bed for a mobile communication system.

As it can be seen at figures above, the developed digital clock synchronization algorithm has been successful using PAM, BPSK and QPSK signals of different channel models at high frequencies. It successfully follows the alternating phase errors changing in time. In the digital versions of the feed-back algorithms, number clock oscillator is used instead of the voltage control oscillator (VCO) used in analog systems. The tests performed – using high frequency channel models – both on Matlab platform and on the TMS320C6701 digital signal processor has revealed that our decision feedback model has been successful. According to these results, if the zero's are not nearing to the unit circle the equalization algorithm works very effectively. This is due to the fact that, when the zero's are nearer to the unit circle inverse system stability suffers. At this situation for the stability of the system the transition time need to be prolonged and the preamble information parts need to be increased.Channel equalization and clock synchronization algorithms of the current receiver modem structures shall be improved to provide higher performance when new algorithms are developed for these functions. For the developments we used TMS320C6701 digital signal processor for real time application. The TMS320C6701 processor draws too much current which makes it unsuitable for mobile applications where batteries are used as the power source. In such cases the processor could be replaced with a TMS320C54x family processor. The signal processing techniques used in transmitter and receiver modems are not single. Various algorithms can be adapted to different situations. For instance, turbo error coding techniques, blind equalization techniques and Viterbi decoder can be used to improve performance [10-13].

REFERENCES

1. Meyr, H., Ascheid, G., Synchronization in Digital Communications, **John Wiley and Sons**, 1990.
2. Bergmans., Jan W.M., Digital Base band Transmission and Recording, **Kluwer Academic Publishers**, Boston, 1996**.**
3. **NATO STANAG** 4285, Characteristics of 1200/2400/3600 bits per second single tone modulators/demodulators for HF radio links, 1990.
4. Tomasi, W., Advanced Electronic Communications Systems, **Prentice Hall**, Englewood Cliffs, N.J., 1992.
5. Bingham, J.A.C., The Theory and Practice of Modem Design, **John Wiley and Sons**, New York, 1988.
6. Warnes., P., 1999, Hunt Engineering Heron 1 Heron Processing Module for C6201 & C6701 User Manual Harware Rev A Document Rev D, **Hunt Engineering**.
7. Tanyer, S.G., Sert, M. ve Çınar, E., Sayısal İşaret Analiz Sınıflandırma ve Ters-Kipleme Sisteminin Geliştirilmesi, **IEEE Sinyal İşleme ve Uygulamaları Kurultayı**, Bildiriler Kitabı s. 387-391, Antalya, 2000.
8. M. Oerder and H. Meyr, **Digital Filter and Square Timing Recovery**, IEEE Trans, Commun., vol. COM-36, pp. 605-612, May 1988.
9. Andy Bateman, **Digital Communications**, Addison-Wesley, 1999.
10. Athanasios A. Rontogiannis, Sergios Theodoridis, On inverse factorization adaptive least-squares algorithms, **Elsevier Signal Processing**, 52 (1996), 35-47.
11. Yu, S.-J., Direct blind channel equalization via the programmable canonical correlation analysis, **Elsevier Science Signal Processing**, Aug 2001, p. 1715-1724.
12. Hui, L., Guanghan, X., Lang, T., Kailath, T., Recent developments in blind channel equalization: From cyclostationarity to subspaces, **Elsevier Science Signal Processing**, April 1996, p. 83-99.
13. Sinha, A., Das, P.K., Basu, D., Implementation and timing analysis of Clock Syncronization on a transputer-based replicated system, **Elsevier Science Information and Software Technology**, Jan 1998, p. 291-309.
14. Baykal, B., Constantinides, A.G., A neural approach to the Underdetermined-Order Recursive Least-Squares Adaptive Filtering, **Elsevier Science Neural Networks**, November 1997, p. 1523-1531.